# Storage Register Design for an Ion Trap Quantum Processor

A thesis for the degree

Bachelor of Science

at

Leibniz Universität Hannover

Felix Springer

April, 2021

# Abstract

A scalable ion trap quantum processor requires the storage of ions. This thesis provides a design for an external linear storage register based on the surface-electrode ion trap. The thesis also provides the procedures of shuttling ions and merging ions in and out of the register. A recommended design using symmetric RF electrodes and an ion distance of 120µm is elaborated.

**Keywords:** quantum information processing, ion storage register, trapped ions, ion transport, near-field microwaves

## Declaration of Authorship

I declare that I composed this thesis myself. All of the used sources and materials are listed. References and citations have been marked. This thesis has not been submitted, neither in whole nor in parts, to any examination committee.

**Felix Springer**, April 7, 2021

**Supervisor:** Prof. Dr. Christian Ospelkaus

# Contents

# Chapter 1

# Introduction

Quantum information processing, as proposed by Deutsch [Deu85, p. 113], has the potential to outperform classical computers. Trapped ions are one of the most promising platforms for quantum processors to date[1]. Grover's [Gro97] and Shor's [Sho94] algorithm have been implemented with actual quantum computers [Fig+17; Mon+16]. The current goal is to achieve quantum supremacy [HM17; Zho+20].

## 1.1 Surface electrode ion trap

An ion trap uses the electromagnetic field to confine the location of charged particles. A common example is the Paul trap [PS53], which is a quadrupole ion trap.

A surface electrode ion trap uses planar electrodes to trap an ion above a "chip" [Bro+15, p. 1421]. This currently researched approach[2] is used to implement scalable ion trap quantum processors.

## 1.2 Intent of this thesis

The goal of this thesis is to design a storage register using surface electrode ion traps. Aside from the fundamental constraints and optimizations a lot of design decisions will be justified by the decisions that were already made by the research group "Trapped-Ion Quantum Engineering" at the "Institute of Quantum Optics" at "Leibniz Universität Hannover".

The storage register should be able to adiabatically store ions for as long as possible and also provide methods for moving the ions inside the register and merging single ions in and out of the register. Furthermore, the ion register should be designed as compact as possible to trap large numbers of ions in a small space.

[1] Olm+07; Sch+13; Har+14; Wan+17; Bru+19; Hol+20.
[2] Hah19; Hol19; Hol+20; Zar+19.

# Chapter 2

# Designing a storage register

One possible solution to implement a storage register is a periodic arrangement of surface electrode ion traps.

## 2.1 Axial confinement with DC electrodes

A proven design for the DC electrode structure is a two-dimensional array of potential wells [Hol+20]. To simplify this design, a one-dimensional array will be the first step towards a storage register.

For now the confinement in the $y$- and $z$-direction will be ignored, to focus on the arrangement of DC electrodes. The goal for the DC electrodes will be a periodic structure along the $x$-axis. This will result in equidistant potential wells which can be seen in figure 2.1. The distance between the ions will be called $w_{\text{trap}}$.

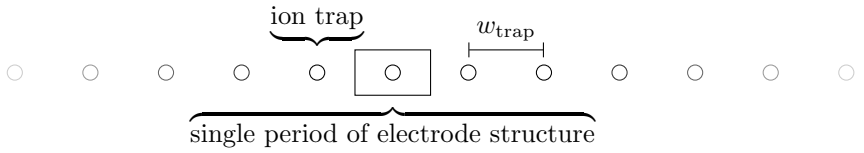


Figure 2.1: The periodic structure of potential wells in one dimension can be seen by looking at the equidistant positions of ions. $w_{\text{trap}}$ is the distance of two neighboring ions and also the width of a single period of the electrode structure. A single period of the DC electrode structure can be seen magnified in figure 2.2.

The next step is to decide on the number and shape of the DC electrodes. With two electrodes per ion it would be possible to create the desired potential wells, but to allow for transport of the ions in the $x$-direction one more electrode is necessary.

A very basic design could look somewhat like figure 2.2. This design is similar to the DC electrodes for the two-dimensional linear trap array from Holz et al. [Hol+20, p. 4]. 3 different voltages will be used for the whole storage register and the adiabatic transport will be performed on all potential wells simultaneously.

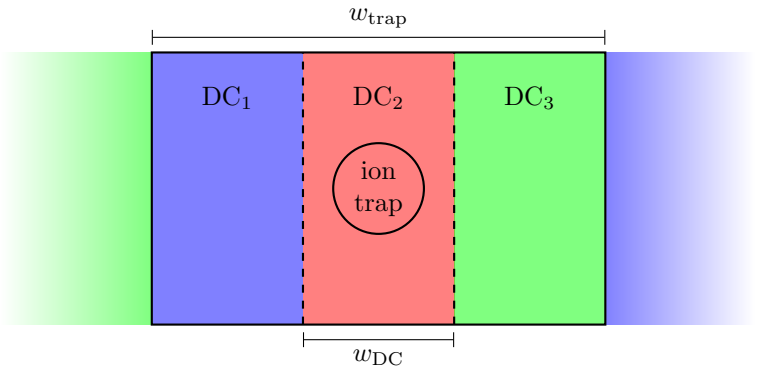


Figure 2.2: The most basic periodic DC electrode structure allowing for ion transport uses 3 electrodes per ion. The ions are separated by distance $w_{\text{trap}}$ and each electrode has length $w_{\text{DC}}$.

This design completely ignored the $y$- and $z$-confinement until now, which will be addressed below.

## 2.2 Spatial confinement with RF and DC electrodes

To achieve confinement in the $y$- and $z$-direction RF electrodes parallel to the $x$-axis will be used. The DC electrode design will have to accommodate some space for that.

The RF electrodes can go either in the center [Hah19, p. 72; Ung20, p. 16], splitting the DC electrodes apart, or outside of the DC electrodes [Hol+20, p. 2]. These two different electrode structures are visualized in figure 2.3 and 2.4.

Figure 2.3 is a modified version of figure 2.2, where the asymmetric RF region is right in the center of the DC electrodes. The split DC electrodes are symmetrically identical and the depth in $y$-direction is given by $d_{\text{DC}}$. The ion trapping position is centered between the DC electrodes, which are 456µm apart. The exact setup of the asymmetric RF region is explained in a section A.3 and figure A.1 visualizes, why this design is called asymmetric.

The design in figure 2.4 will be referred to as the symmetric RF design. This design simply uses two RF electrodes on outside of the DC electrodes with a distance of $d_{\text{DC}}$ and a width of $d_{\text{RF}}$.

This is in general a simpler configuration than the asymmetric design, as there is no asymmetry in the RF electrodes here. The gradient of the pseudopo-

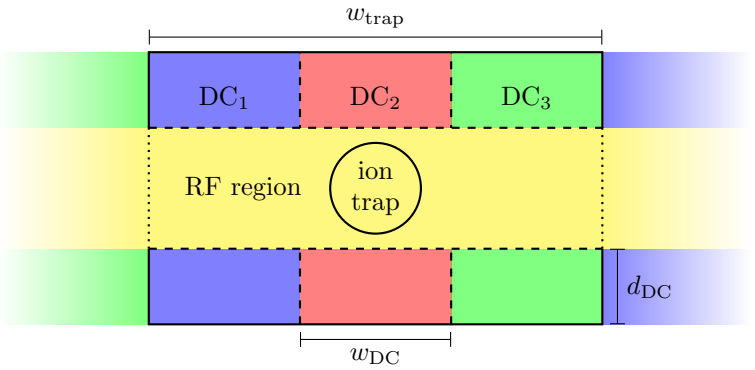


Figure 2.3: This figure extends figure 2.2. The DC electrodes are split up into two parts each, making space for the asymmetric RF electrode structure in the center. The DC electrode pairs have an equal distance to the trap center, defined by the size of the RF region. The depth of each of the DC electrode pairs is given by $d_{\text{DC}}$. The RF region is explained more in depth in section A.3.

tential, introduced in section 2.2.2, should automatically cancel out regarding the $y$-direction.

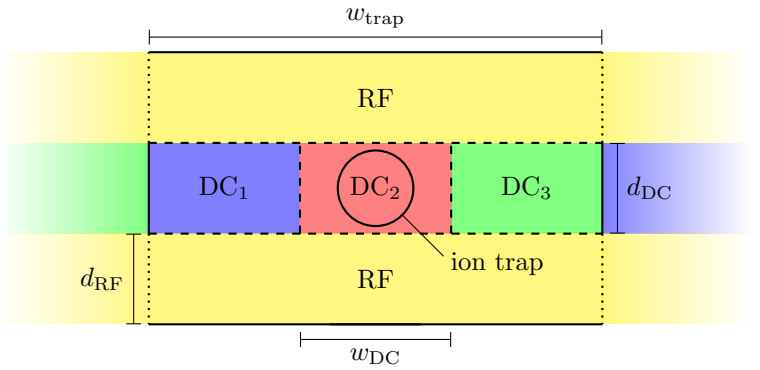


Figure 2.4: This figure extends figure 2.2. The two RF electrodes are placed around the DC electrodes and powered with the same voltage. The depth of the DC and RF electrodes is given by $d_{\text{DC}}$ and $d_{\text{RF}}$ respectively.

### 2.2.1 Electrostatic potential $\phi_{\text{DC}}$

To calculate the electrostatic potential $\phi_{\text{DC}}$, generated by the DC electrodes, equation 2.1 is used [Hou08, p. 4]. Here $\binom{x_1}{y_1}$ and $\binom{x_2}{y_2}$ describe two diagonal corners of the rectangular DC electrodes.

$$\begin{aligned}\phi_{\text{DC}}(x,y,z) = \frac{U}{2\pi}\Bigg( &\arctan\left[\frac{(x_1-x)(y_1-y)}{z\sqrt{z^2+(x_1-x)^2+(y_1-y)^2}}\right] \\ &-\arctan\left[\frac{(x_1-x)(y_2-y)}{z\sqrt{z^2+(x_1-x)^2+(y_2-y)^2}}\right] \\ &-\arctan\left[\frac{(x_2-x)(y_1-y)}{z\sqrt{z^2+(x_2-x)^2+(y_1-y)^2}}\right] \\ &+\arctan\left[\frac{(x_2-x)(y_2-y)}{z\sqrt{z^2+(x_2-x)^2+(y_2-y)^2}}\right]\Bigg)\end{aligned} \tag{2.1}$$

For non-rectangular electrodes a closed-form expression like equation 2.1 hasn't been found, but the electrostatic potential $\phi_{\text{DC}}$ can still be calculated numerically with equation 2.1 [Hou08, p. 4].

### 2.2.2 Pseudopotential $\phi_{\text{RF}}$

The pseudopotential $\phi_{\text{RF}}$ [Hou08, p. 3] will be viewed as constant over time. The pseudopotential is calculated from the angular frequency $\omega$ of the ion and the electric field $E(t) = -\nabla\phi(t)$, where the time-dependent potential $\phi(t)$ is calculated with equation 2.1. Equation 2.2 gives a formula for $\phi_{\text{RF}}$ using the

charge number $Z$ of the trapped ion, the elementary charge $e$ and the ion mass $m$.

$$\phi_{\mathrm{RF}} = \frac{Z^2 e^2}{4m\omega^2} ||E||^2 \tag{2.2}$$

### 2.2.3 Total potential $\phi_{\mathrm{total}}$

The total potential $\phi_{\mathrm{total}}$ is the sum of the pseudopotential $\phi_{\mathrm{RF}}$ of the RF electrodes and the electrostatic potential $\phi_{\mathrm{DC}}$ generated by the DC electrodes.

$$\phi_{\mathrm{total}} = \phi_{\mathrm{RF}} + \phi_{\mathrm{DC}} \tag{2.3}$$

Just like the pseudopotential $\phi_{\mathrm{RF}}$, the total potential $\phi_{\mathrm{total}}$ will be viewed as a static potential for timespans $\Delta t \gg \Omega$.

The total potential $\phi_{\mathrm{total}}$ will be subject to further analysis and will be abbreviated with $\phi$ in the following sections. In particular the dependence on control variables such as the DC voltages $U_i$, axial frequency $\Omega$, DC electrode width $w_{\mathrm{DC}}$ and number of DC electrodes $N$ are used to find an electrode configuration best suited for actual use.

An example for a particular set of control variables can be seen in figure 2.5.

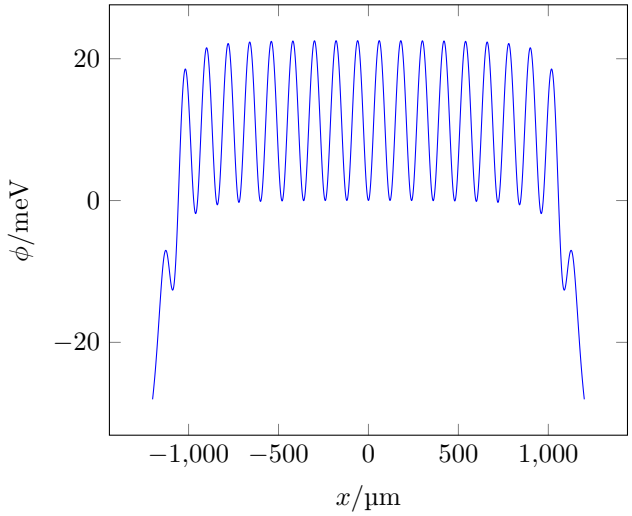


Figure 2.5: The potential $\phi(x)$ provides equidistant potential wells on the $x$-axis for an axial frequency of $\Omega = 3\mathrm{MHz}$ and a DC electrode width of $w_{\mathrm{DC}} = 40\mu\mathrm{m}$ with $N = 3$ DC electrodes per ion. This is a simulation of a symmetric RF design with $d_{\mathrm{DC}} = 60\mu\mathrm{m}$ and $d_{\mathrm{RF}} = 120\mu\mathrm{m}$ using 57 DC electrodes. The DC electrodes use voltages $U_1 = U_3 = -0.554\mathrm{V}$ and $U_2 = 0.536\mathrm{V}$.

## 2.3 Calculating DC voltages $U_i$ to trap ions

To trap an ion, the electric field at the trapping position should vanish.

$$\nabla\phi = E = 0 \tag{2.4}$$

The trapping position in the $y$-$z$-plane is given by the default trapping position of the RF electrodes without DC electrodes $U_i = 0$. The $x$ value for the position is variable, but the one closest to the center well is used, to reduce the effects of the finite size of the storage register. Because of the symmetry of the DC electrodes along the $x$-axis, the electric field in $y$-direction will cancel out, thus $E_y = 0$.

With three DC voltages $U_1$, $U_2$ and $U_3$, there are three degrees of freedom, which need to be resolved. Two degrees of freedom are determined by equation 2.4 with $E_x = 0$ and $E_z = 0$. The remaining degree of freedom is resolved by specifying the axial frequency $\Omega$.

$$\Omega = \frac{1}{2\pi}\sqrt{\frac{Ze}{m}\partial_x\partial_x\phi} \tag{2.5}$$

Solving equation 2.4 and 2.5 for $U_i$ will give an exact solution for $N = 3$ DC voltages.

## 2.4 Shuttling ions with adiabatic transport

To move the ions back and forth inside the register a procedure for ion shuttling needs to be implemented. Adiabatic transport for surface electrode ion traps has been suggested and implemented before [Hol+20; Ung20]. The procedure described here is the simultaneous movement of all ions in the storage register, keeping the distance $w_{\text{trap}}$ between them.

Calculating the DC voltages $U_i$ is done by solving the constraints from section 2.3 at the $x$-position of the ion transport.

In figure 2.6 it can be observed, that the voltages $U_i$ are shifted versions of each other. This relation comes from the fact, that the DC electrode structure, can be seen as periodic on a distance of $w_{\text{DC}}$ for a long enough storage register. The exact relation is recursively given by equation 2.6 or explicitly by equation 2.7

$$U_i(x) = U_{i+1}(x + w_{\text{DC}}) \tag{2.6}$$

$$U_i(x) = U_1(x - (i-1)w_{\text{DC}}) \tag{2.7}$$

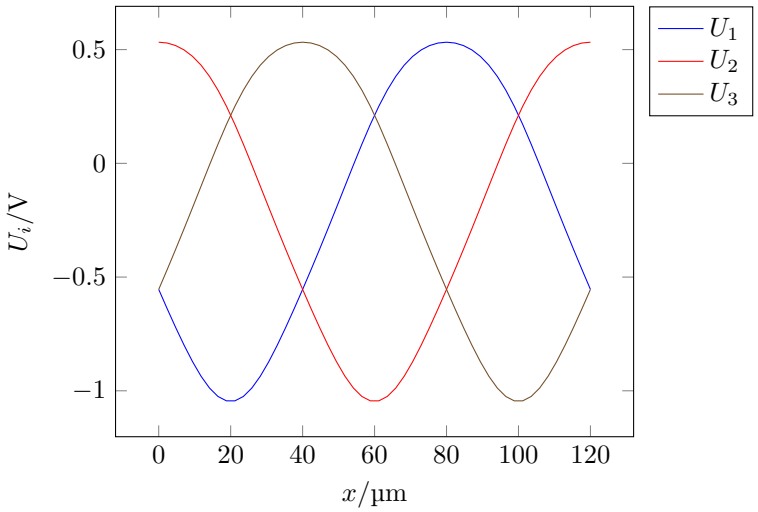


Figure 2.6: The voltages $U_i$ for $N = 3$ DC electrodes are displayed for the adiabatic transport by one period on the $x$-axis of the storage register. The variable $x$ in this plot refers to the position of the potential wells. The control variables used in this plot are the same as in figure 2.5.

## 2.5 Reviewing performance indicators

The trap depth $\phi_\Delta$, the maximum absolute voltage $U_{\max}$ and the natural frequencies $\omega_i$ are important parameters to decide on a suitable trap configuration.

### 2.5.1 Trap depth $\phi_\Delta$

The trap depth $\phi_\Delta$ is the difference in potential $\phi$ between a minimum and it's next maximum. Therefore it is also the minimal energy necessary for an ion to leave the trap, regarding each position of the potential wells.

The escape point is calculated numerically and the difference in potential $\phi$ at the trap center and the escape point gives the trap depth $\phi_\Delta$.

### 2.5.2 Maximum voltage $U_{\max}$

The maximum voltage $U_{\max}$ is the maximum absolute voltage during the ion shuttling.

$$U_{\max} = \max_{x \in [0, w_{\text{trap}}]} |U_1(x)| \tag{2.8}$$

Granted that the storage register is large enough equation, 2.8 doesn't need to account for $U_i$ with $i > 1$, since on the interval $[0, w_{\text{trap}}]$ the voltages $U_i$ can be represented in terms of $U_1$ with equation 2.7.

The maximum voltage $U_{\max}$ needs to be kept low enough for actual hardware to be able to provide it, but also still high enough, so that electromagnetic noise doesn't interfere with the ion trapping.

A lower maximum voltage $U_{\max}$ is also desirable to reduce the electromagnetic noise generated by the DC electrodes.

### 2.5.3 Natural frequencies $\omega_i$

Just like the axial frequency given by equation 2.5, there are two more normal modes of the potential $\phi$. These can be calculated with eigenvalues and eigenvectors of the Hessian matrix $H_\phi$ evaluated at the trapping positions.

The eigenvectors $v_i$ construct an orthonormal basis. For an eigenvector $v_i$ with eigenvalue $\lambda_i$ the natural frequency $\omega_i$ in direction of $v_i$ is given by equation 2.9.

$$\omega_i = \frac{1}{2\pi}\sqrt{\frac{Ze}{m}\lambda_i}\ , \qquad i = x, y, z \tag{2.9}$$

For the natural frequencies $\omega_i$, it will be desirable, that their scale and direction are kept somewhat stable during the ion shuttling.

The orthonormal basis constructed by the eigenvectors can be compared to the standard basis. The angle $\angle_i$ between a standard basis vector $e_i$ and its corresponding eigenvector $v_i$ during ion shuttling indicate the rotation of the axes. Small angles indicate stable ion shuttling.

$$\angle_i = \arccos \frac{e_i \cdot v_i}{||e_i||\ ||v_i||}$$

To allow a simple comparison between control parameters, the maximum angle

$$\angle_{\max} = \max_{i\in\{x,y,z\}} \left\{ \max_{x_\mathrm{t}\in[0,w_\mathrm{trap}]} \angle_i(x_\mathrm{t}) \right\}$$

gives a good performance indicator. $x_\mathrm{t}$ gives the ion trapping positions during the shuttling and determines, where to evaluate the Hessian matrix $H_\phi$.

## 2.6 Optimizing width $w_{\mathrm{DC}}$ and depth $d_{\mathrm{DC}}$ of DC electrodes

In this section the previously explained performance indicators $\phi_\Delta$, $U_{\max}$ and $\omega_i$ will be used to find the best set of control variables $w_{\mathrm{DC}}$, $d_{\mathrm{DC}}$, $U_i$ and $\Omega$ for both the symmetric and asymmetric RF electrode design with $N = 3$ DC electrodes per potential well.

The following analysis is performed for $^9\mathrm{Be}^+$ ions, which determine the mass $m \approx 9.012\mathrm{u}$ [Mei+16] and the electric charge $Z \cdot e = e$. Both RF designs use the same radial angular frequency and voltage from equation 2.2

$$\omega = 2\pi \cdot 88.191\mathrm{MHz} \ \text{ and } \ U_{\mathrm{RF}} = 75\mathrm{V}.$$

### 2.6.1 Symmetric RF design

The symmetric RF design, which is visualized in figure 2.4, is parametrized by the width $w_{\mathrm{DC}}$ and depth $d_{\mathrm{DC}}$ of the DC electrodes and the depth $d_{\mathrm{RF}}$ of the RF electrodes.

The RF electrode depth in this section will be kept set to $d_{\mathrm{RF}} = 120\mu\mathrm{m}$ with a distance of $d_{\mathrm{DC}} = 60\mu\mathrm{m}$. This results in a trapping height of $z \approx 67.1\mu\mathrm{m}$.

The following calculations are performed for the center most well.

#### Maximum voltage $U_{\mathrm{max}}$

In the symmetric RF design the trapping position is right above the DC electrodes. This results in a very strong effect of the static potential $\phi_{\mathrm{DC}}$ on the ion. Because of this, the voltages $U_i$ necessary to trap an ion are quite low, which can also be seen in figure 2.7. They can even be so low, that it could become hard to supply these voltages accurately, as for example with $\Omega = 1\mathrm{MHz}$.

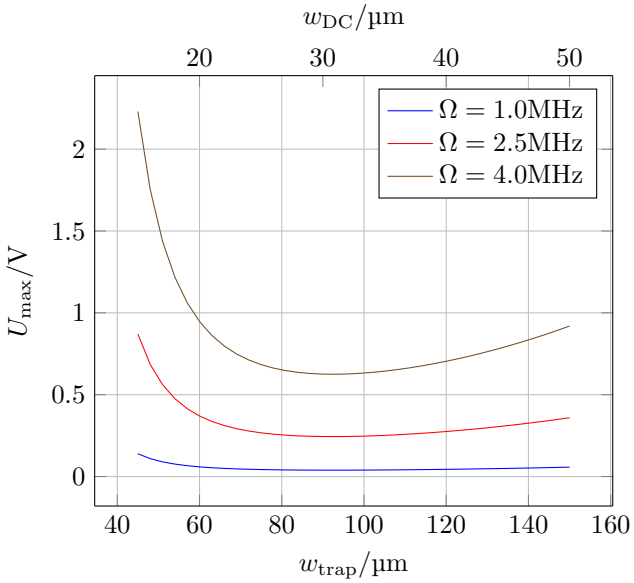


Figure 2.7: The maximum voltage $U_{\mathrm{max}}$ is displayed for the symmetric RF design from figure 2.4. The graphs show the dependence on the trap width $w_{\mathrm{trap}} = N \cdot w_{\mathrm{DC}}$ for some reasonable axial frequencies $\Omega$. $U_{\mathrm{max}}$ is minimal for a trap width of $w_{\mathrm{trap}} = 93\mu\mathrm{m}$ and independent of the axial frequency $\Omega$.

#### Trap depth $\phi_\Delta$

The escape point in the symmetric RF design lies on the $x$-axis for reasonable trap widths $w_{\mathrm{trap}} \ll 1000\mu\mathrm{m}$. This means, that the static potential $\phi_{\mathrm{DC}}$

has a strong influence on the trap depth $\phi_\Delta$, due to the low distance between electrodes and ions.

The relation between the trap width $w_{\text{trap}} = N \cdot w_{\text{DC}}$ and the trap depth $\phi_\Delta$ can be observed in figure 2.8. For small trap widths $w_{\text{trap}}$ the trap depth $\phi_\Delta$ is quite low, but increasing the axial frequency $\Omega$ also increases the trap depth. With higher axial frequencies $\Omega$, the resulting maximal voltage $U_{\text{max}}$ will also increase, but this is still fine, since the voltages are quite low in this trap design. Since the lowest DC electrode width currently achievable is about $w_{\text{DC}} \approx 20\mu\text{m}$ due to fabrication limitations, the axial frequency $\Omega$ should be chosen with that in mind.

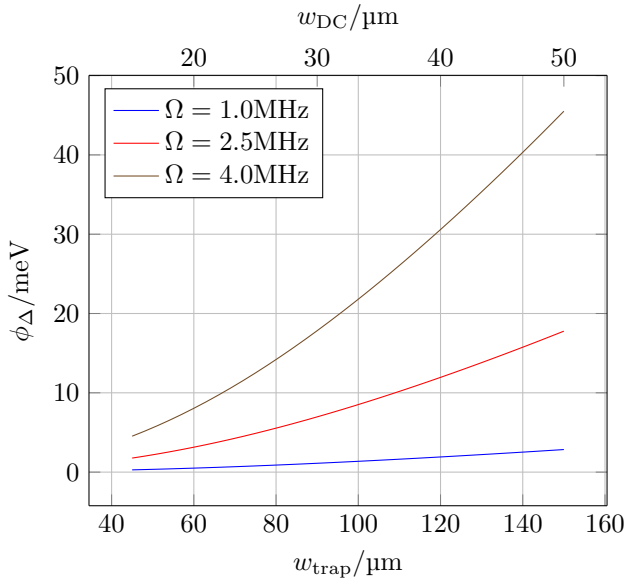


Figure 2.8: The relation between trap depth $\phi_\Delta$ and trap width $w_{\text{trap}} = N \cdot w_{\text{DC}}$ is displayed for some reasonable axial frequencies $\Omega$. Larger trap depths $\phi_\Delta$ occur for greater trap widths $w_{\text{trap}}$ and greater axial frequencies $\Omega$.

### Natural frequencies $\omega_i$

The natural frequency in $\omega_x$ is constrained by equation 2.5.

The maximum rotation angle $\angle_{\text{max}}$ between the eigenvectors of the Hessian matrix $H_\phi$ and the canonical basis vectors is displayed in figure 2.9.

Small rotations, such as these, shouldn't effect the trapped ions and still provide an adiabatic transport.

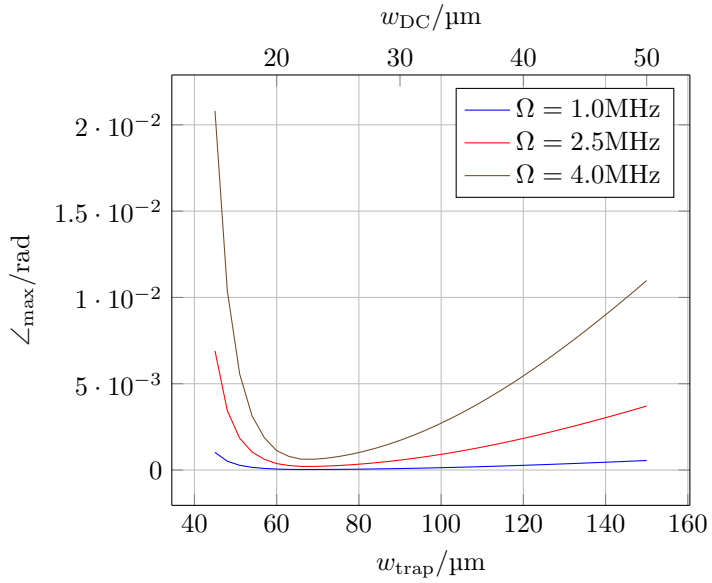


Figure 2.9: The maximum rotation angle $\angle_{\max}$ is displayed in relation to the trap width $w_{\mathrm{trap}}$ for various axial frequencies $\Omega$. The rotation angles are quite low for all of the displayed trap widths $w_{\mathrm{trap}}$.

### 2.6.2 Asymmetric RF design

Just like the symmetric RF design, the asymmetric RF design is parametrized by the width $w_{\mathrm{DC}}$ and depth $d_{\mathrm{DC}}$ of the DC electrodes, as shown in figure 2.3. The effect of the DC electrode depth $d_{\mathrm{DC}}$ is very small compared to the width $w_{\mathrm{DC}}$ as long as $d_{\mathrm{DC}}$ is large enough. In this section $d_{\mathrm{DC}} = 200\mu\mathrm{m}$ is used. The RF region is explained in depth in section A.3.

#### Maximum voltage $U_{\max}$

The maximum voltage $U_{\max}$ is a very limiting factor, when it comes to this design. Since the distance from the ion trap to the DC electrodes is larger than in the symmetric design, the voltages $U_i$ are also greater. The exact relation between the maximum voltage $U_{\max}$ and the trap width $w_{\mathrm{trap}}$ can be observed in figure 2.10.

For a practical design it will be desirable to choose $U_{\max}$ to be minimal. In figure 2.6.2 this minimum is located at $w_{\mathrm{trap}} = 795\mu\mathrm{m}$ and independent of the axial frequency $\Omega$.

It is unfortunate, that using this design results in even higher voltages $U_{\max} \gg 10\mathrm{V}$ when trying small DC electrode widths $w_{\mathrm{DC}} < 100\mu\mathrm{m}$. When using higher voltages, the electromagnetic noise might also effect other parts of a quantum processor.

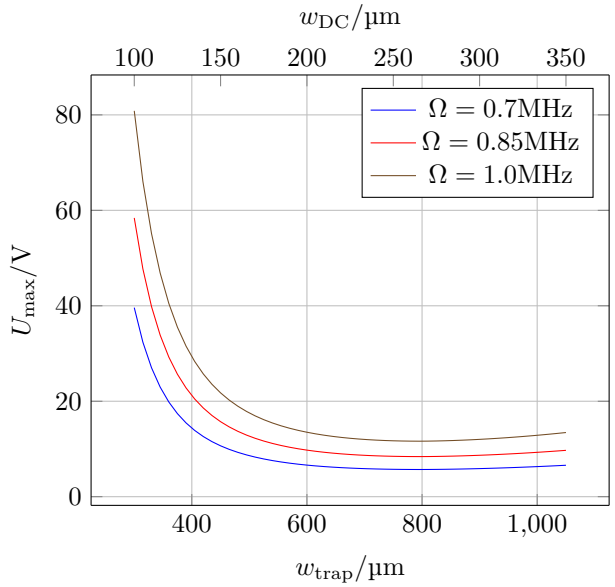


Figure 2.10: The maximum voltage $U_{\mathrm{max}}$ is displayed for the asymmetric RF design from figure 2.3. The graphs show the dependence on the trap width $w_{\mathrm{trap}} = N \cdot w_{\mathrm{DC}}$ for some reasonable axial frequencies $\Omega$. $U_{\mathrm{max}}$ is minimal for a trap width of $w_{\mathrm{trap}} = 795\mu\mathrm{m}$ and independent of the axial frequency $\Omega$.

#### Trap depth $\phi_\Delta$

The trap depth is not limited by the electrostatic potential $\phi_{\mathrm{DC}}$ generated by the DC electrodes. The escape point lies in the radial plane instead and is determined mainly by the RF electrode design, further explained in section A.3.

## 2.7 Merging ions in and out of the storage register

This section proposes a method to merge single ions in and out of the register. The register used in this section is using the symmetric RF electrode design with $d_{\mathrm{RF}} = 120\mu\mathrm{m}$, $d_{\mathrm{DC}} = 60\mu\mathrm{m}$, $w_{\mathrm{DC}} = 40\mu\mathrm{m}$ and $\Omega = 3\mathrm{MHz}$. The merge region is designed very similar to the rest of the register, using DC electrodes with the same width $w_{\mathrm{DC}}$ and depth $d_{\mathrm{DC}}$, but with specifically addressable voltages.

After the merge region another storage register is used for moving an ion using the adiabatic transport described in section 2.4. This second register's purpose is just the transport of a single ion and it could be replaced with an approach similar to [Ung20, p. 22].

The voltages for the DC electrodes of these two registers are calculated as described in section 2.3. Together with the relation 2.7 the voltages are fully parametrized by $U_1$ displayed in figure 2.11.

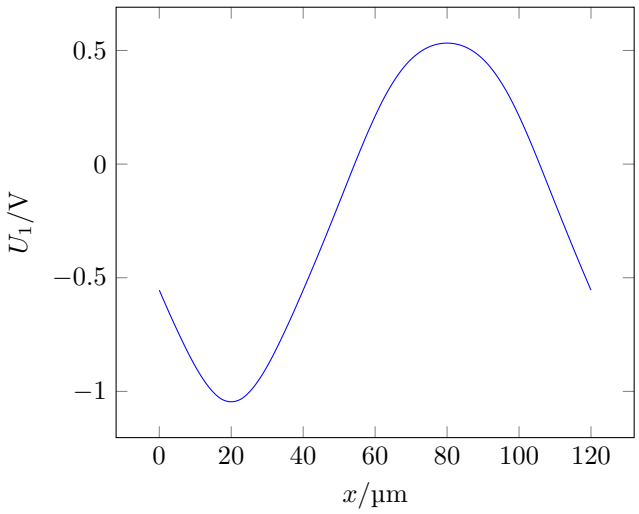


Figure 2.11: The voltage $U_1$ is displayed in relation to the $x$-value during the adiabatic transport. This voltage parametrizes all other regular voltages $U_i$ and transport voltages $U_{\mathrm{t}i}$. Parameters for this solution are a symmetric RF design with $d_{\mathrm{RF}} = 120\mu\mathrm{m}$ and a periodic 3 DC electrode structure with $d_{\mathrm{DC}} = 60\mu\mathrm{m}$, $w_{\mathrm{DC}} = 40\mu\mathrm{m}$ and $\Omega = 3\mathrm{MHz}$.

With this design the most important decision is, how many DC electrodes to control with individual voltages $U_{\mathrm{m}j}$, where $j = 1, \ldots, N_{\mathrm{merge}}$. An example for a merge region using $N_{\mathrm{merge}} = 1$ individually controlled DC electrodes is displayed in figure 2.12. Additional individually controlled DC electrodes $\mathrm{DC}_{\mathrm{m}j}$ extend the merge region by replacing adjacent transport electrodes $\mathrm{DC}_{\mathrm{t}i}, i = 1, 2, 3$.

During idle operation and when shifting all of the register at once, all DC electrodes are simply controlled with the same voltages. During these operations the merging electrodes are addressed in groups of maximum three with

$$j' - 1 \equiv (j - 1) \mod 3.$$

The resulting voltages are parametrized by equation 2.10.

$$U_i = U_{\mathrm{t}i} = U_{\mathrm{m}j'} \tag{2.10}$$

When merging an ion into or out of the register, the electrodes of the register are supplied with the default voltages $U_i(x = 0)$. The transport electrodes have a voltage of $U_{\mathrm{t}i} = U_i(x)$, where $x$ is the ion position relative to the last regular ion trap in the idle register.

The individually controlled voltages $U_{\mathrm{m}j}(x)$ will be accounted for in the following.

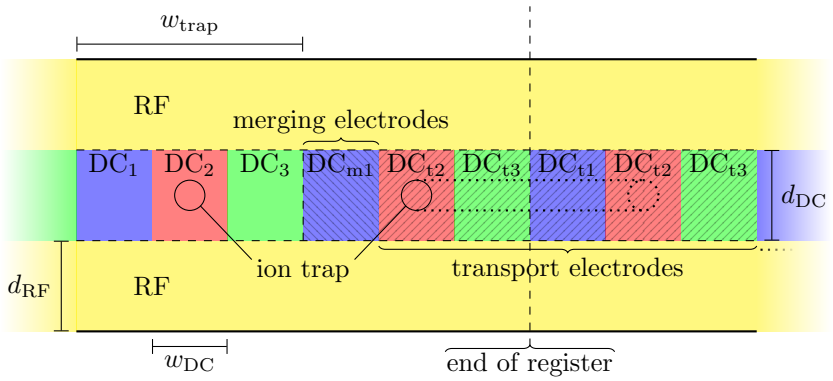


Figure 2.12: This figure shows the electrode configuration for a merge region with symmetric RF electrodes. The left side show the regular storage register constructed by the electrodes $\text{DC}_i, i = 1, 2, 3$. On the right side are the electrodes, which handle the transport from and to the register, $\text{DC}_{\text{t}k}, k = 1, 2, 3$. In the center is the merge region with $N_{\text{merge}} = 1$ separately controlled electrodes $\text{DC}_{\text{m}j}, j = 1, \ldots, N_{\text{merge}}$. The dotted line and circle show the path an ion takes during merging in and out of the register. The center circle represents the last ion position of the regular storage register.

### 2.7.1 No individually controlled voltages ($N_{\text{merge}} = 0$)

The trivial configuration is to avoid the merge region altogether. This approach doesn't work very well for small DC electrode widths $w_{\text{DC}} \ll 50\mu\text{m}$, because during the merging procedure, the last potential well in the storage register becomes deformed and thus the ion won't be stored adiabatically.

The deformation has the strongest impact on the trap depth at a merging distance between $\frac{1}{2}w_{\text{trap}}$ and $2w_{\text{DC}} = \frac{2}{3}w_{\text{trap}}$. This can be explained by a new potential well being created right next to an existing one, which brings the trap depth in the $x$-axis down and the ion might be lost. This phenomenon can be seen in figure 2.13.

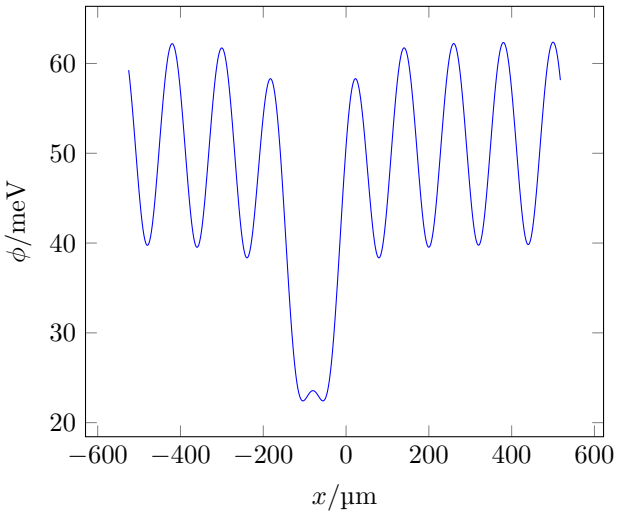


Figure 2.13: Here the potential $\phi$ is displayed for an idle storage register performing the merging procedure with $N_{\text{merge}} = 0$ merging electrodes. The merging distance on display is $2 \cdot w_{\text{DC}}$. The storage register is configured using a symmetric RF design with $d_{\text{RF}} = 120\mu\text{m}$ and a periodic 3 DC electrode structure with $d_{\text{DC}} = 60\mu\text{m}$, $w_{\text{DC}} = 40\mu\text{m}$ and $\Omega = 3\text{MHz}$. The trap depth at $x = -w_{\text{trap}}$ is lower than for the other potential wells.

### 2.7.2 Avoid disruptive potential well ($N_{\text{merge}} = 1$)

When adding individual voltages $U_{\text{m}i}$, there are many ways to calculate these voltages.

The voltage $U_{\text{m1}}$ can be set to a constant in the second half of the merging process. This will keep both the last ion in the register and the merging ion trapped.

Another evident option is to set the voltage $U_{\text{m1}}$ to the mean value of the neighboring electrodes during the second half of the merging process.

$$U_{\text{m1}}(x) = \frac{U_3(x) + U_{\text{t2}}}{2}$$

With these simple approaches an optimal solution will unfortunately not be found, which is why they won't be discussed any further. The voltage $U_{\text{m1}}$ can instead be optimized by calculating the trap depths $\phi_\Delta$ for any merging distance $x$. This addresses the trap depth $\phi_\Delta$ of the merging potential well and the last well remaining in the register.

Since the calculation of the trap depth is very CPU-intensive, the resolution of the solution is quite low, which can also be seen in figure 2.14.

When comparing figure 2.13 and 2.15 it becomes apparent, that this procedure involving $N_{\text{merge}} = 1$ is far superior.

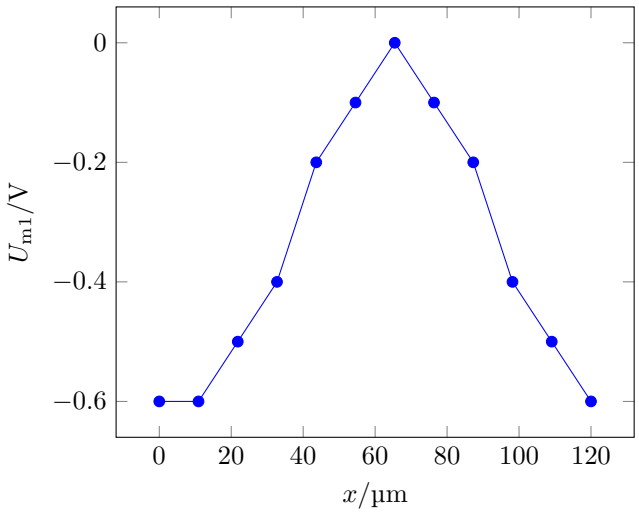


Figure 2.14: The voltage $U_{\mathrm{m1}}$ is displayed in relation to the merging distance $x$. The storage register is configured using a symmetric RF design with $d_{\mathrm{RF}} = 120\mu\mathrm{m}$ and a periodic 3 DC electrode structure with $d_{\mathrm{DC}} = 60\mu\mathrm{m}$, $w_{\mathrm{DC}} = 40\mu\mathrm{m}$ and $\Omega = 3\mathrm{MHz}$.

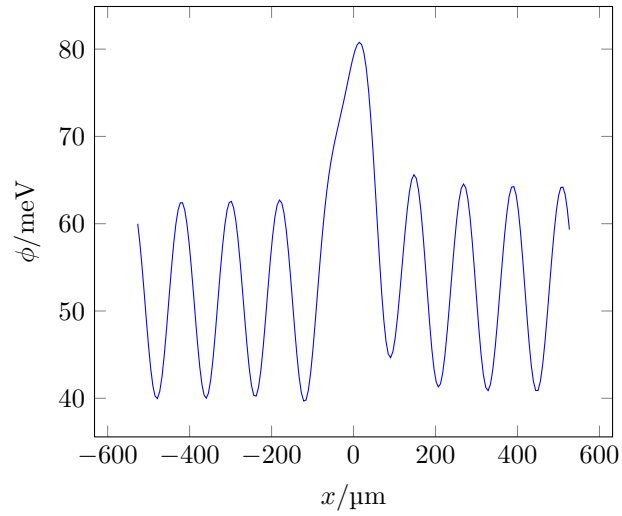


Figure 2.15: Here the potential $\phi$ is displayed for an idle storage register performing the merging procedure with $N_{\mathrm{merge}} = 1$ merging electrodes. The merging distance on display is $2 \cdot w_{\mathrm{DC}}$. The storage register is configured using a symmetric RF design with $d_{\mathrm{RF}} = 120\mu\mathrm{m}$ and a periodic 3 DC electrode structure with $d_{\mathrm{DC}} = 60\mu\mathrm{m}$, $w_{\mathrm{DC}} = 40\mu\mathrm{m}$ and $\Omega = 3\mathrm{MHz}$.

### 2.7.3 Solving exactly ($N_{\mathbf{merge}} = 6$)

To make sure the axial frequency $\Omega$ stays constant, constraints as in section 2.3 can be used. When applied to the merging ion and the last ion in the register, $N_{\mathrm{merge}} = 6$ degrees of freedom can solve the 6 equations. This approach leads to solutions, which unfortunately deform the next potential wells in the register so much, that ions trapped in these wells would be lost.

In general all attempts, that involved exact solving for merging voltages $U_{\mathrm{m}i}$, resulted in deformed potentials.

# Chapter 3

# Conclusion

## 3.1 Comparing the symmetric and asymmetric RF design

With the objectives described in section 2.5 the symmetric RF design greatly outperforms the asymmetric design.

Assuming reasonable voltages $U_{\max} \lesssim 10\text{V}$, the symmetric design can be used with a trap width $w_{\text{trap}}$ roughly 10 times smaller than the asymmetric design.

The trap depth $\phi_\Delta$ is not the critical point of concern for either design, when it comes to ion shuttling at least.

The natural frequencies rotate only in negligible amounts for the symmetric design.

The natural frequencies have not been analyzed for the asymmetric design due to the higher priority of continuing with the symmetric design.

## 3.2 A recommended design

According to the criteria discussed in this thesis, one of the best confirmed configurations can be summarized:

**Symmetric RF electrodes:**

- RF electrode depth $d_{\text{RF}} = 120\mu\text{m}$

**Periodic DC electrodes:**

- DC electrodes per period $N = 3$
- DC electrode width $w_{\text{DC}} = 40\mu\text{m}$
- DC electrode depth $d_{\text{DC}} = 60\mu\text{m}$
- Number of merging electrodes $N_{\text{merge}} = 1$

**Control parameters:**

- Axial frequency $\Omega = 3\text{MHz}$
- Radial angular frequency $\omega = 2\pi \cdot 88.191\text{MHz}$
- RF electrode voltage $U_{\text{RF}} = 75\text{V}$
- $^{9}\text{Be}^{+}$-ions with charge number $Z = 1$ and mass $m \approx 9.012\text{u}$

The layout of the merge region is displayed in figure 2.12. The processes of shuttling and merging are implemented by the voltages displayed in figure 3.1 and figure 3.2.

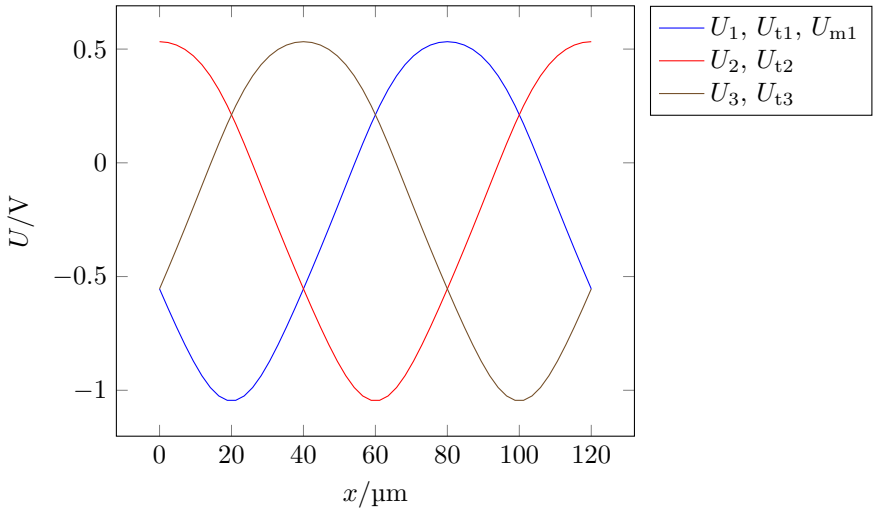


Figure 3.1: The full set of DC voltages are displayed for ion shuttling using the recommended parameters from section 3.2.

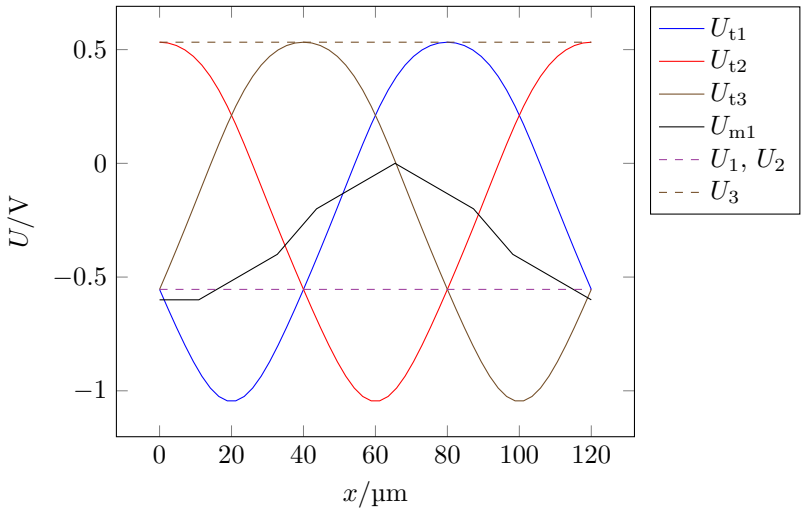


Figure 3.2: The full set of DC voltages are displayed for the merging process using the recommended parameters from section 3.2.

## 3.3 Outlook

### 3.3.1 Attaching a junction

To make use of the proposed storage register design, it will be necessary to attach it to an X-junction [Osp+11; Ung20]. The merging process described in section 2.7 can provide the core part of the procedure. Repeated execution of that procedure can move the last ion arbitrarily far away from the register.

Moving the extracted ion from the periodic DC electrode structure into the junction should be the next step to attach the register. The most apparent solution for this would be to have a region of individually controlled DC electrodes to change from the periodic transport potential, visible in figure 2.15, to a single well ion trapping potential.

### 3.3.2 Time-dependent ion transport

This thesis used the ion position to implement ion transport. In an experimental environment the ion position isn't a control parameter, so the shuttling and merging procedures have to be executed with a dependency on time $t$ instead of position $x$.

This time-dependency can be realized with a monotonic function

$$\theta : [0, t_{\max}] \to [0, w_{\text{trap}}]$$

using boundary conditions $\theta(0) = 0$ and $\theta(t_{\max}) = w_{\text{trap}}$. This can then be used to calculate the voltages $U_i(\theta(t))$, $U_{\text{m}j}(\theta(t))$ and $U_{\text{t}i}(\theta(t))$.

The simplest solution would therefore be a linear function

$$\theta_{\text{linear}}(t) = \frac{w_{\text{trap}}}{t_{\max}} \cdot t.$$

Maybe a spline interpolation with additional constraints, such as

$$\dot{\theta}(0) = \dot{\theta}(t_{\max}) = 0$$

will provide even better results.

With a full design, surface electrode chips can be produced and heating rates $\Gamma_h$ [Hol+20, p. 2] can then be measured. Aside from testing the parameters of the storage register, an optimized function $\theta$ using a small time interval $[0, t_{\max}]$ can be found experimentally.

Aside from implementing a prototype, there are other ideas, that might improve the storage register.

### 3.3.3 Possible improvements

#### Additional DC voltages

Using more than 3 DC voltages per ion can possibly improve the trap depth $\phi_\Delta$ and the natural modes $\omega_i$.

This is only worth exploring, when the fabrication limit regarding the DC electrode width $w_{\text{DC}}$ proves to be unachievable. Because otherwise this approach would significantly increase the trap width

$$w_{\text{trap}} = N \cdot w_{\text{DC}}.$$

I tried 4 and 5 DC electrodes with the asymmetric RF region, as explained in section A.4. This might provide more interesting results for the symmetric RF design.

#### Improving the merge region

The design of the merge region is quite simple. Especially the decision of using the same DC electrode width $w_{\text{DC}}$ has the drawback, that the ion density in the register is limited by the trap depth $\phi_\Delta$ during the merging process.

A design, that works independently of the rest of the register, should also allow a smaller trap width $w_{\text{trap}}$ and thus a higher ion density.

When making attempts towards this improvement, an optimization regarding the trap depth might provide good results, as this approach was also favorable with the simple design provided in this thesis.

Increasing the number of individually controlled merging electrodes $N_{\text{merge}}$ to 2 or 3 might already give significantly better results.

### Improving the end of the register

In figure 2.5 one can already see that the potential wells close to the end of the register are deformed. Adding a merge region already fixes this problem, which can be seen in figure 2.15. At some point the register will have to end and adding an individual DC electrode might improve the potential in that area.

This is not a critical point of failure, since this will just bring down the number of ions the register can hold. There are also other ideas to greatly improve the number of ions.

### 2-dimensional register designs

A 1-dimensional storage register design will likely not be the fastest way to access specific ions, depending on the position in the register. 2-dimensional designs, such as a grid- or tree-like designs will improve this. This will also drastically increase the number of ions that can be trapped per area.

The single arms of these 2-dimensional designs can probably use a design very similar to the one proposed in this thesis.

# Appendix A

## A.1 Calculation caveats

When calculating the properties of the total potential $\phi$ for specific potential wells, one should keep in mind, that the actual potential wells might be shifted slightly from the presumed position. This is the case, because even when using many DC electrodes and very long RF electrodes, some minor asymmetries will become apparent. I had problems when calculating the trap depth $\phi_\Delta$ in particular.

To resolve this issue, it is recommended to first calculate the actual position of the potential well by finding a minimum starting from the assumed position.

All electrodes were approximated without gaps between them. Actual manufacturing requires small gaps in the range of 4.5µm [OWC14, p. 181] or 9µm [Hol+20, p. 8], depending on the production.

## A.2 Differences to a linear trap array

A two-dimensional linear trap array as proposed by Holz et al. [Hol+20] is not just a storage register for ions. Here the quantum operations are performed while the ions stay in the array, unlike the approach which is suggested in this thesis.

This brings up a lot more properties to be desired for the ion traps. To perform motional coupling in particular, the ions need to be either rather close to each other with a distance of about 40µm or special operations of moving specific neighboring ions closer to each other need to be implemented [Hol+20, p. 2]. This smaller distance also results in an increased heating rate $\Gamma_h$ [Hol+20, p. 2].

Another additional downside of this proposal is, that laser-addressing of individual trapping sites is necessary for single qubit operations [Hol+20, p. 3].

## A.3 Asymmetric RF region

The asymmetric RF region is part of the design of the ConsTrap by Hahn [Hah19]. It is using a meander-like microwave conductor (MWM) and an additional RF electrode [Hah19, p. 72]. In addition to this an MWS electrode is used. The RF electrodes provide the pseudopotential $\phi_{\mathrm{RF}}$. The layout is visualized in figure A.1.

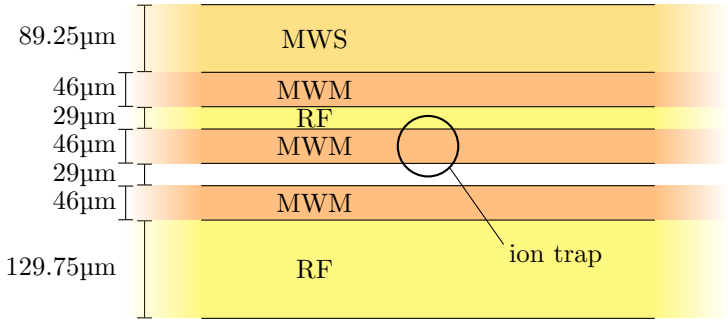


Figure A.1: The asymmetric RF region uses 3 different kinds of electrodes, which are RF, MWM and MWS electrodes. The ion trapping axis is located at the suggested ion trapping position.

The radial trap depth generated by this asymmetric RF region is

$$\phi_{\Delta(\mathrm{radial})} = 28.2\mathrm{meV}$$

at a trapping height of

$$z \approx 70.8\mu\mathrm{m}.$$

## A.4 Periodic design with more than 3 voltages

I tested designs with 4 and 5 DC voltages in combination with the asymmetric RF region.

In figure A.4 it can be observed, that increasing the number of DC electrodes per period results in lower voltages. In comparison to the symmetric RF the voltages are still very high, in particular when taking the DC electrode width $w_{\mathrm{DC}}$ into account.

Since the results were not too promising and due to time limitations I wasn't able to investigate this any further.

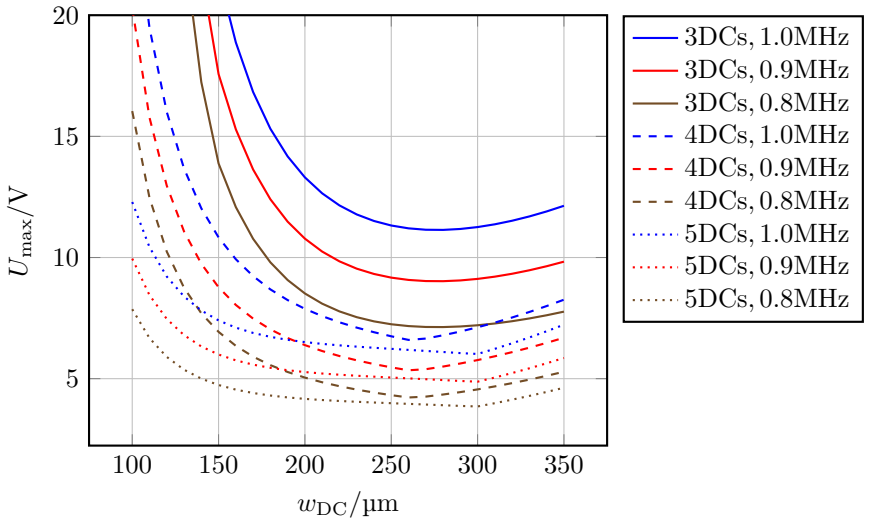


Figure A.2: The maximum absolute voltage $U_{\max}$ during the adiabatic transport is displayed in relation to the width of the DC electrodes $w_{\mathrm{DC}}$ for different numbers of DC electrodes per ion (3, 4, 5) and different axial frequencies each (1.0MHz, 0.9MHz, 0.8MHz) for the asymmetric RF design.
It is notable that, for each number of DC electrodes per ion, the optimal width $w_{\mathrm{DC}}$ is constant when varying the axial frequency.

## A.5 Software and calculations

All calculations were performed using "Wolfram Mathematica 12.1" from the proprietor "Wolfram Research". A lot of source code from the "Institute of Quantum Optics" at "Leibniz Universität Hannover" was reused.

Plotting and writing was done with "TeX Live", licensed under free software licenses, including the LPPL[1] and GPLv2[2].

[1] LaTeX Project Public License
[2] GNU General Public License, version 2

# List of Figures

# Bibliography


[Bro+15] M. Brownnutt et al. "Ion-trap measurements of electric-field noise near surfaces". In: *Reviews of Modern Physics* 87.4 (Dec. 2015), pp. 1419–1482. DOI: 10.1103/revmodphys.87.1419.

[Bru+19] Colin D. Bruzewicz et al. "Trapped-ion quantum computing: Progress and challenges". In: *Applied Physics Reviews* 6.2 (June 2019), p. 021314. DOI: 10.1063/1.5088164.

[Deu85] D. Deutsch. "Quantum theory, the Church-Turing principle and the universal quantum computer". In: *Proceedings of the Royal Society of London. A. Mathematical and Physical Sciences* 400.1818 (July 1985), pp. 97–117. DOI: 10.1098/rspa.1985.0070.

[Fig+17] C. Figgatt et al. "Complete 3-Qubit Grover search on a programmable quantum computer". In: *Nature Communications* 8.1 (Dec. 2017). DOI: 10.1038/s41467-017-01904-7.

[Gro97] Lov K. Grover. "Quantum Mechanics Helps in Searching for a Needle in a Haystack". In: *Physical Review Letters* 79.2 (July 1997), pp. 325–328. DOI: 10.1103/physrevlett.79.325.

[Hah19] Henning Hahn. "Two-qubit microwave quantum logic gate with $^{9}Be^{+}$ ions in scalable surface-electrode ion traps". PhD thesis. Gottfried Wilhelm Leibniz Universität Hannover, July 2019.

[Har+14] T. P. Harty et al. "High-Fidelity Preparation, Gates, Memory, and Readout of a Trapped-Ion Quantum Bit". In: *Physical Review Letters* 113.22 (Nov. 2014). DOI: 10.1103/physrevlett.113.220501.

[HM17] Aram W. Harrow and Ashley Montanaro. "Quantum computational supremacy". In: *Nature* 549.7671 (Sept. 2017), pp. 203–209. DOI: 10.1038/nature23458.

[Hol+20] Philip C. Holz et al. "2D Linear Trap Array for Quantum Information Processing". In: *Advanced Quantum Technologies* 2000031 (Sept. 2020). DOI: 10.1002/qute.202000031.

[Hol19] Philip Christoph Holz. "Towards ion-lattice quantum processors with surface trap arrays". PhD thesis. University of Innsbruck, Nov. 2019.

[Hou08] M. G. House. "Analytic model for electrostatic fields in surface-electrode ion traps". In: *Physical Review A* 78.3 (Sept. 2008). DOI: 10.1103/physreva.78.033402.

[Mei+16] Juris Meija et al. "Atomic weights of the elements 2013 (IUPAC Technical Report)". In: *Pure and Applied Chemistry* 88.3 (Mar. 2016), pp. 265–291. DOI: 10.1515/pac-2015-0305.

[Mon+16] T. Monz et al. "Realization of a scalable Shor algorithm". In: *Science* 351.6277 (Mar. 2016), pp. 1068–1070. DOI: 10.1126/science.aad9480.

[Olm+07] S. Olmschenk et al. "Manipulation and detection of a trapped $Yb^+$ hyperfine qubit". In: *Physical Review A* 76.5 (Nov. 2007). DOI: 10.1103/physreva.76.052314.

[Osp+11] C. Ospelkaus et al. "Microwave quantum logic gates for trapped ions". In: *Nature* 476.7359 (Aug. 2011), pp. 181–184. DOI: 10.1038/nature10290.

[OWC14] Christian Ospelkaus, Ulrich Warring, and Yves Colombe. "Quantenlogik mit gefangenen Ionen - Qubits in der Mikrowelle". In: *Physik Unserer Zeit* 45.2 (Mar. 2014), pp. 72–78. DOI: 10.1002/piuz.201301358.

[PS53] Wolfgang Paul and Helmut Steinwedel. "Ein Neues Massenspektrometer Ohne Magnetfeld". In: *Zeitschrift für Naturforschung A* 8.7 (July 1953), pp. 448–450. DOI: 10.1515/zna-1953-0710.

[Sch+13] Philipp Schindler et al. "A quantum information processor with trapped ions". In: *New Journal of Physics* 15.12 (Dec. 2013), p. 123012. DOI: 10.1088/1367-2630/15/12/123012.

[Sho94] Peter W. Shor. "Algorithms for quantum computation: discrete logarithms and factoring". In: *Proceedings 35th Annual Symposium on Foundations of Computer Science*. IEEE Comput. Soc. Press, Nov. 1994. DOI: 10.1109/sfcs.1994.365700.

[Ung20] Paul Florian Ungerechts. "Ion Transport for Scalable Quantum Processors". Gottfried Wilhelm Leibniz Universität Hannover, Mar. 2020.

[Wan+17] Ye Wang et al. "Single-qubit quantum memory exceeding ten-minute coherence time". In: *Nature Photonics* 11.10 (Sept. 2017), pp. 646–650. DOI: 10.1038/s41566-017-0007-1.

[Zar+19] G. Zarantonello et al. "Robust and Resource-Efficient Microwave Near-Field Entangling $^9Be^+$ Gate". In: *Physical Review Letters* 123.26 (Dec. 2019). DOI: 10.1103/physrevlett.123.260503.

[Zho+20] Han-Sen Zhong et al. "Quantum computational advantage using photons". In: *Science* 370.6523 (Dec. 2020), pp. 1460–1463. DOI: 10.1126/science.abe8770.